CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a memory core having a plurality of memory cells, a bit line connected to said memory cells, and a sense amplifier connected to said bit line;

a command control circuit for outputting an access request signal for accessing said memory cells in response to an access request supplied through a command terminal;

a refresh timer for generating an internal refresh request at predetermined cycles;

an arbiter for determining order of precedence between an access operation corresponding to said access request and a refresh operation corresponding to said internal refresh request when a conflict occurs between said access request and said internal refresh request, and for sequentially outputting a refresh control signal and an access control signal in accordance with the order of precedence;

an operation control circuit for making said memory core perform an access operation in response to said access control signal, and making said memory core perform a refresh operation in response to said refresh control signal; and

a detecting circuit for outputting a detection signal indicating that said refresh operation is yet to be performed when a new internal refresh request occurs before said refresh operation corresponding to said internal refresh request is performed, said detecting circuit operating in a test mode.

2. The semiconductor memory according to claim 1, further comprising

an external terminal for outputting said detection signal to the exterior of the semiconductor memory.

3. The semiconductor memory according to claim 2, further comprising:

a data terminal that is said external terminal;

a tristate output buffer for outputting read data from said memory cells to said data terminal; and

an output mask circuit for controlling said tristate output buffer in said test mode so as to prohibit output of said read data to said data terminal in response to said detection signal and set said data terminal to a high impedance state.

4. The semiconductor memory according to claim 1, further comprising

a refresh selecting circuit for masking said internal refresh request output from said refresh timer and outputting a test refresh request supplied through an external test terminal, instead of said internal refresh request, to said arbiter in said test mode.

5. The semiconductor memory according to claim 1, wherein

said refresh timer receives, in said test mode, a refresh adjustment signal for changing the cycle of generation of said internal refresh request.

6. A semiconductor memory comprising:

a memory core having a plurality of memory cells, a bit line connected to said memory cells, and a sense amplifier connected to said bit line;

a command control circuit for outputting an access request signal for accessing said memory cells in response to an access request supplied through a command terminal;

a refresh timer for generating an internal refresh request at predetermined cycles;

an arbiter for determining order of precedence between an access operation corresponding to said access request and a refresh operation corresponding to said internal refresh request when a conflict occurs between said access request and said internal refresh request;

an interruption circuit for outputting a refresh interrupting signal upon receiving a next access request within a predetermined period from the completion of said access operation performed with precedence over said refresh operation;

an operation control circuit for starting a refresh operation of said memory core when said arbiter determines to give precedence to said internal refresh request, interrupting said refresh operation in execution upon receiving said refresh interrupting signal, and making said memory core perform an access operation when said arbiter determines to give precedence to said access request; and

an interruption detecting circuit for operating in a test mode and outputting a detecting signal when a refresh operation is interrupted in response to said refresh interrupting signal.

7. The semiconductor memory according to claim 6, further comprising

an external terminal for outputting said detection signal to the exterior of the semiconductor memory.

8. The semiconductor memory according to claim 7, further comprising:

a data terminal that is said external terminal;

a tristate output buffer for outputting read data from said memory cells to said data terminal; and

an output mask circuit for controlling said tristate output buffer in said test mode so as to prohibit output of said read data to said data terminal in response to said detection signal and set said data terminal to a high impedance state.

9. The semiconductor memory according to claim 6, further comprising

a refresh selecting circuit for masking said internal refresh request output from said refresh timer and outputting a test refresh request supplied through an external test terminal, instead of said internal refresh request, to said arbiter in said test mode.

10. The semiconductor memory according to claim 6, further comprising

a word line connected to said memory cells, and wherein

said predetermined period is a period from when said operation control circuit

receives an instruction to start a refresh operation from said arbiter until when activation of said word line is started for the refresh operation.